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at the first level predecode two groups of three bits into two 1 of 8 hot bundles and two groups of two bits into two 1 of 4 hot bundles the slowest predecoder is the 1 of 8 hot which involves sending each true or complementary input in the group of three to four 3 input and gates

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a unit inverter has a 41036 nm wide nmos transistor and an 81072 nm wide pmos transistor hence the unit inverter has an effective resistance of $25 \text{ k}\Omega$ 036 mm $69 \text{ k}\Omega$ and a gate capacitance of 036 mm 072 mm 2 ff 22 ff

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within die channel length variation has a 32575 mV effect on threshold voltage so the threshold voltage has a random distribution with a standard deviation of $\sqrt{75230231}$ mV this increases the expected value of leakage by a factor of $e^{0.031 \ln 10} = 1.22129$ or 6%

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20 solutions 4 one reasonable design consists of xnor functions to check bitwise equality a 16 input and to check equality of the input words and an and gate to choose y or 0 assuming an xor gate has $g_p = 4$ the circuit has $g = 493635340$

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adam harris is an associate in the corporate and capital markets groups of morrison foerster s tokyo office adam received his j d from duke university school of law where he was a senior staff editor for the duke journal of constitutional law public policy
















































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